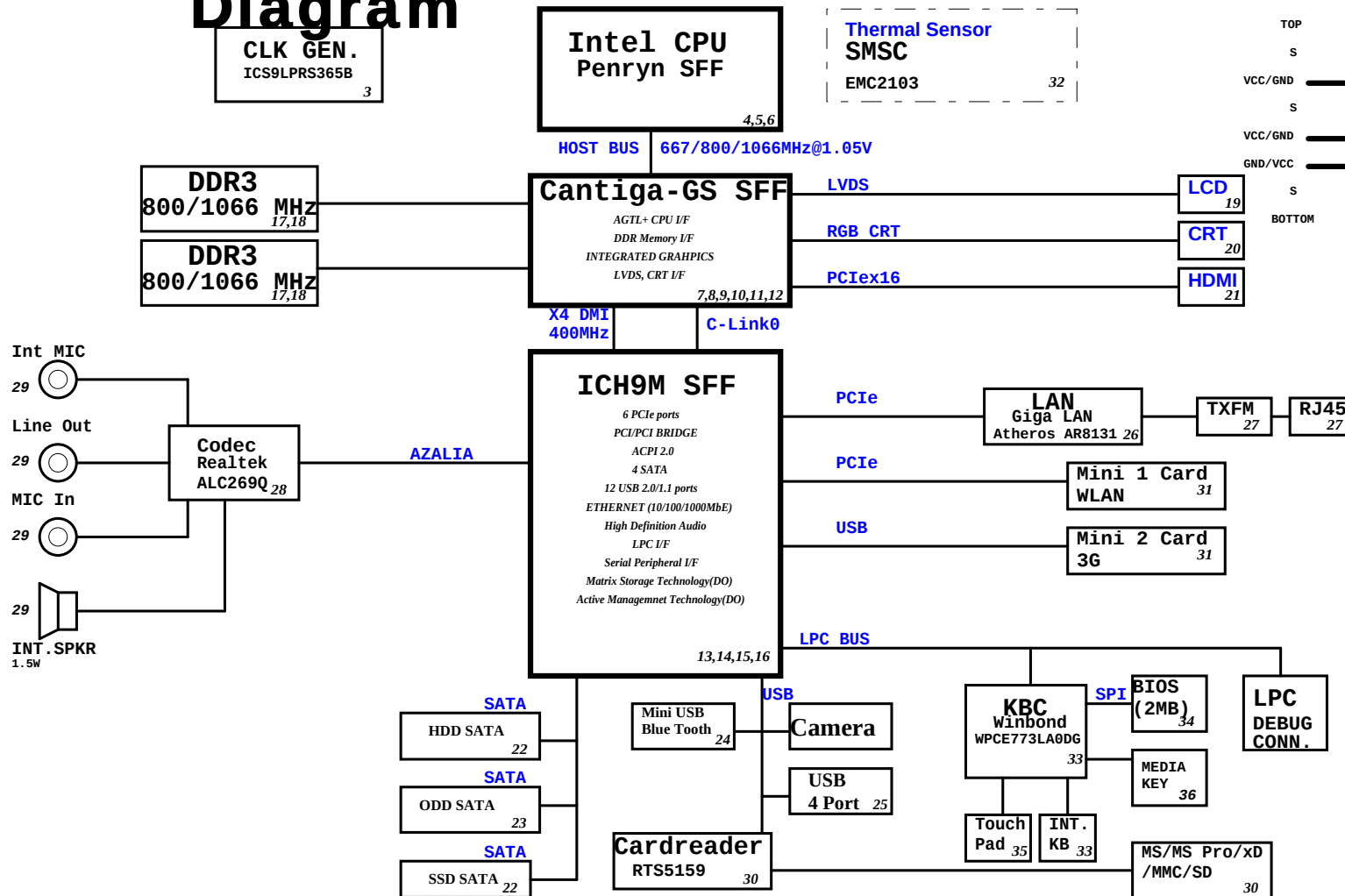


JM41 Block Diagram

Project code: 91.4CQ01.001
PCB P/N : 48.4CQ01.011
REVISION : 08266-1



PCB STACKUP

TOP	_____	L1
S	_____	L2
VCC/GND	_____	L3
S	_____	L4
VCC/GND	_____	L5
GND/VCC	_____	L6
S	_____	L7
BOTTOM	_____	L8

SYSTEM DC/DC TPS51125 36	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5
RT8202 37	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A)
RT8202 38	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(11A)
RT9026 39	
INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 (1.2A)
CHARGER MAX8731A 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
CPU DC/DC ADP3207A 35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 64A
VGA ISL6263A 40	
INPUTS	OUTPUTS
DCBATOUT	VCC GFXCORE (7A)

<Core Design>	
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Title BLOCK DIAGRAM	
Size Custom	Document Number JM41 UMA
Date: Monday, March 09, 2009	Sheet 1 of 40
Rev -1	

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttpot and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

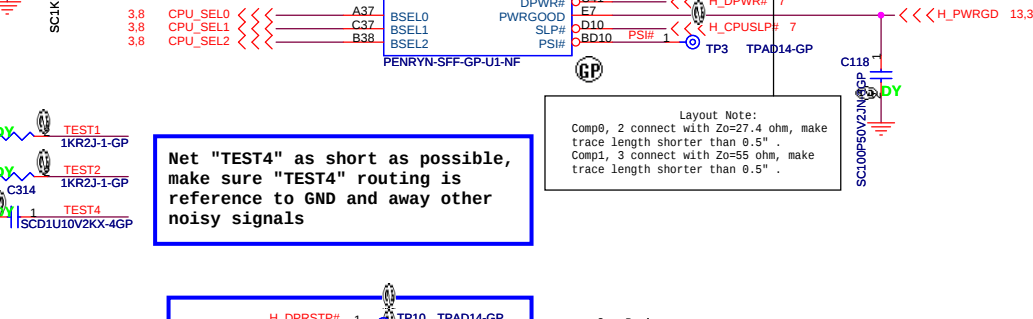
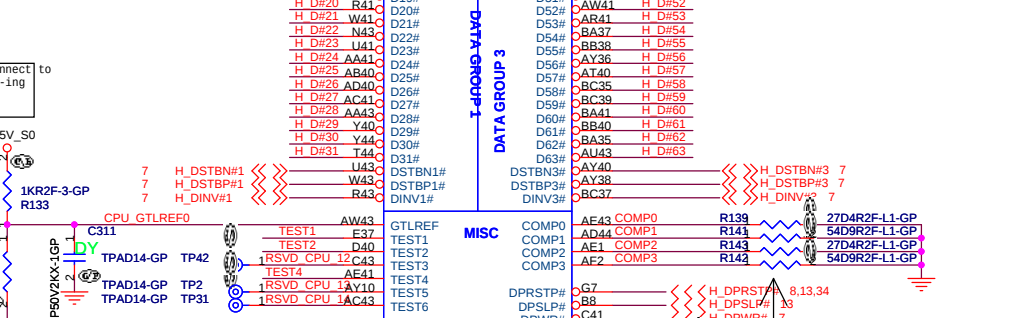
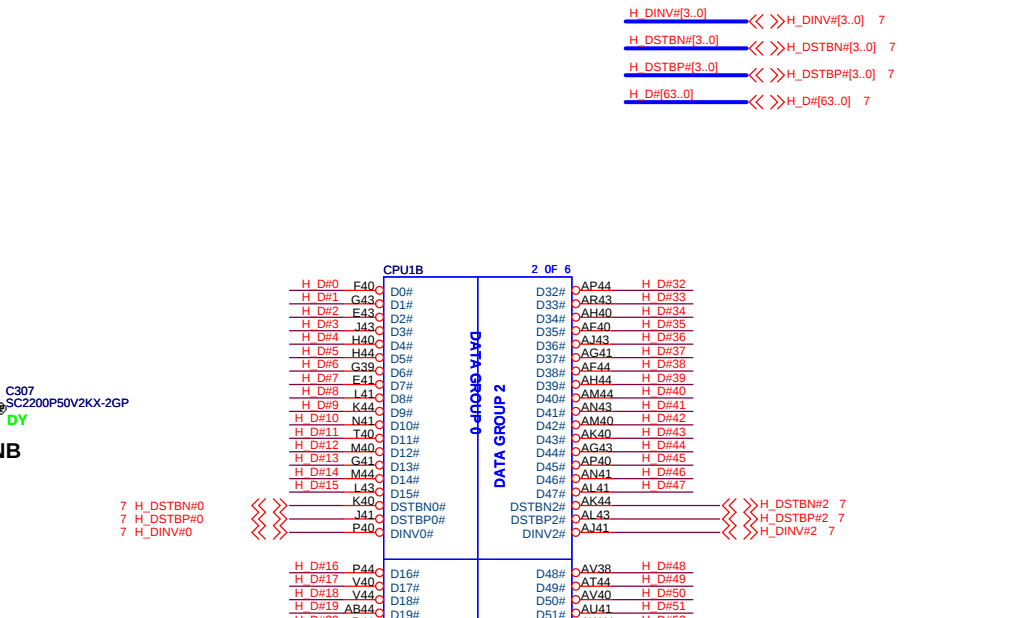
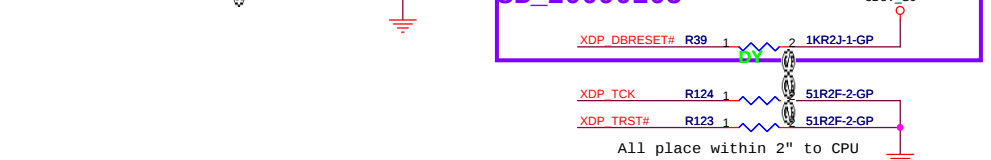
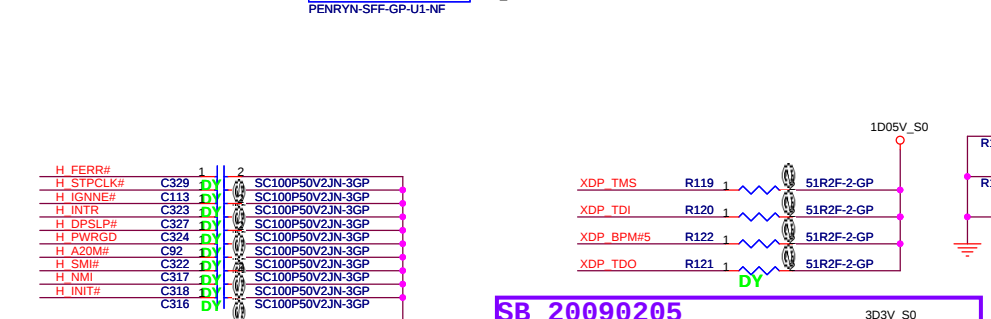
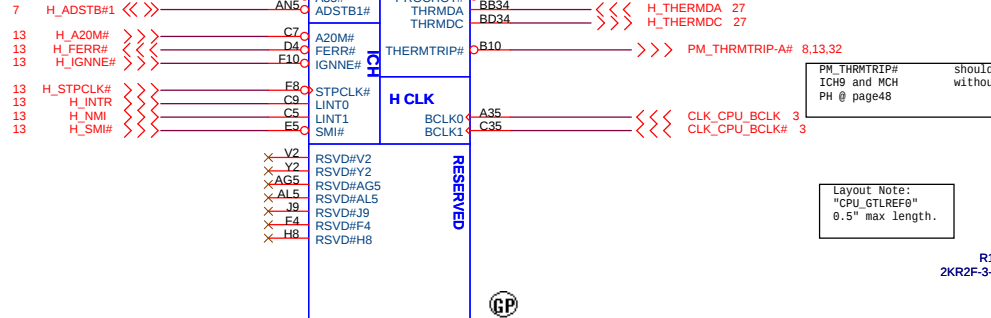
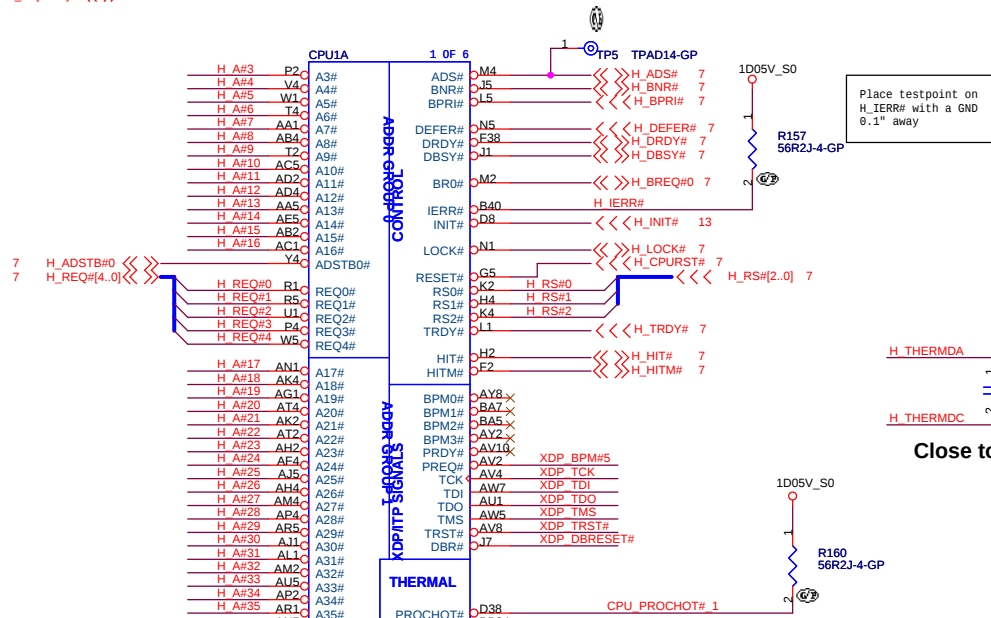
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port 1 = If PCIe is operational, Default) Digital display Port and PCIe are operating simulatanously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIe disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

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Reference			
Size A3	Document Number		Rev
	JM41 UMA		-1
Date: Sunday, March 01, 2009	Sheet 2	of	40

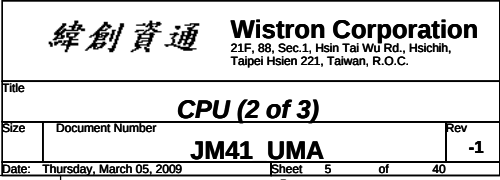
7 H_A#(35..3) <<<>>> H_A#(35..3)

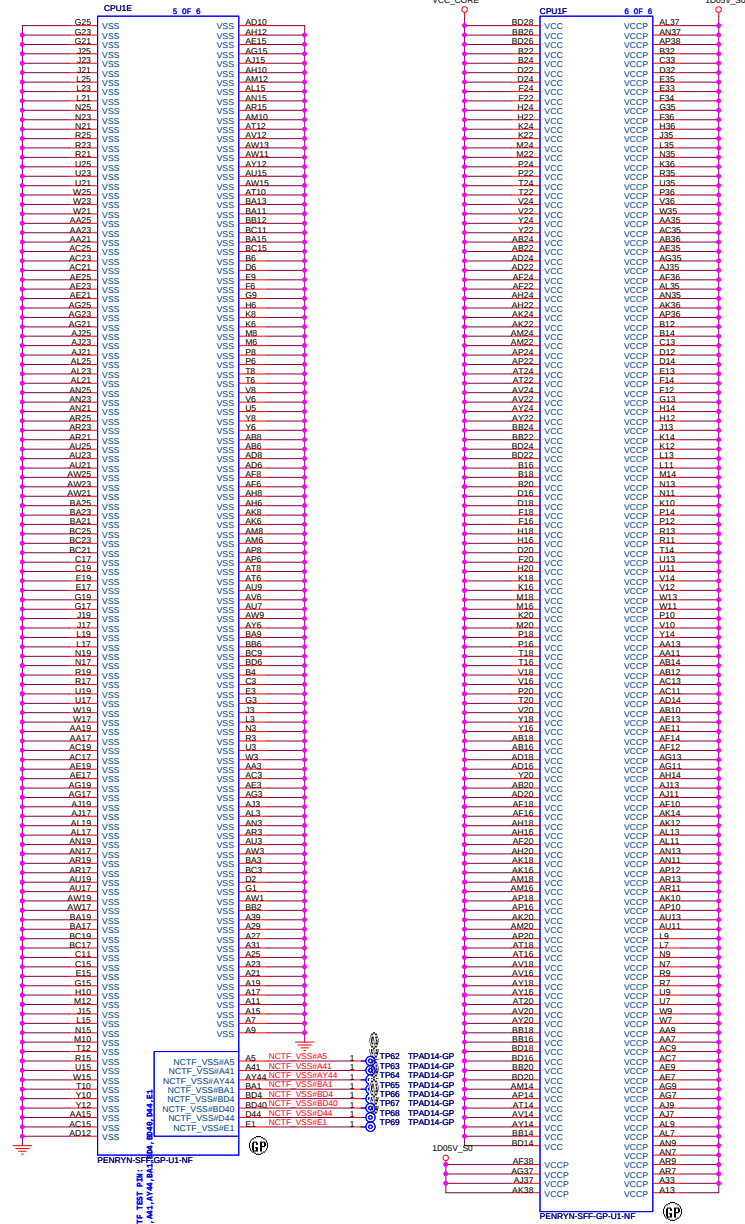


Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

Place these TP on button-side, easy to measure.

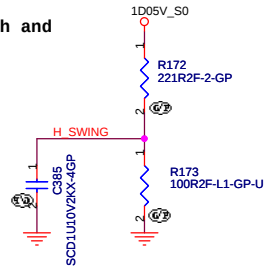
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".



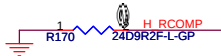


H_SWING routing Trace width and Spacing use 10 / 20 mil

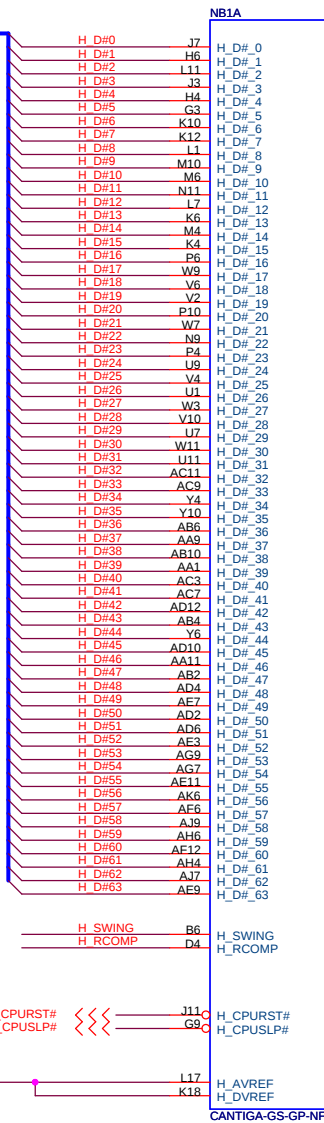
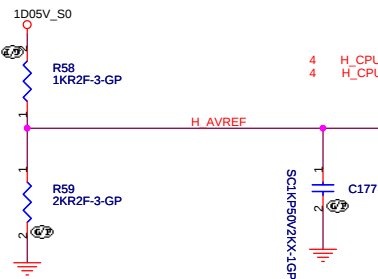
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



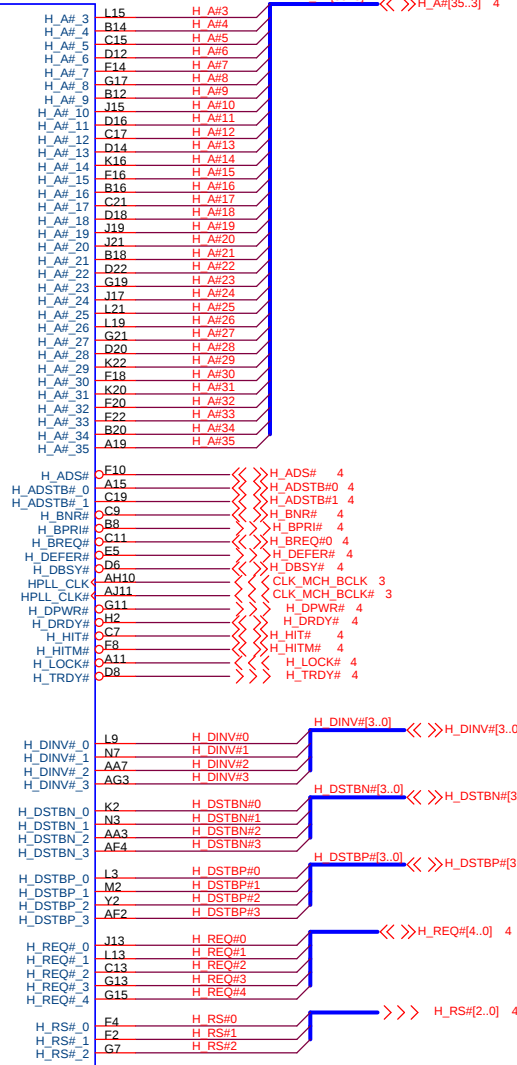
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

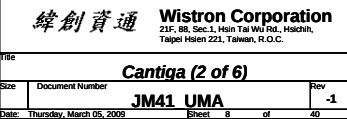


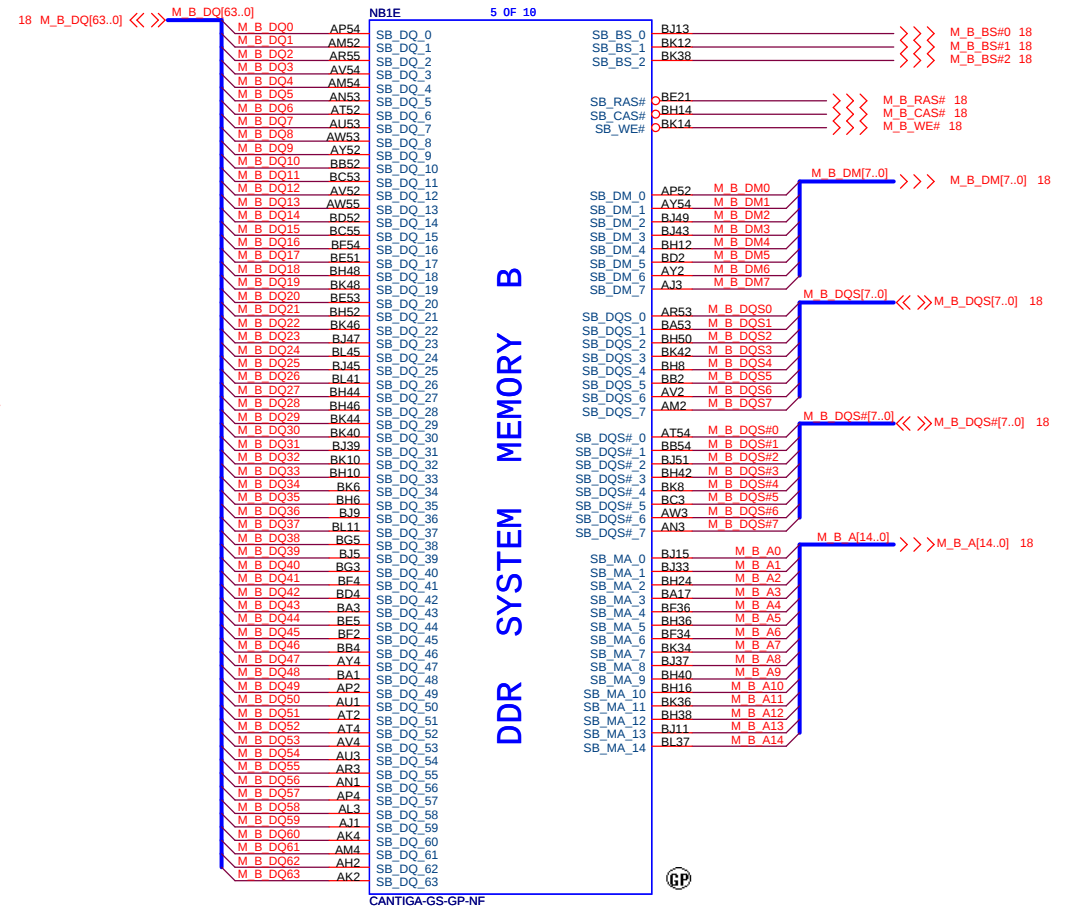
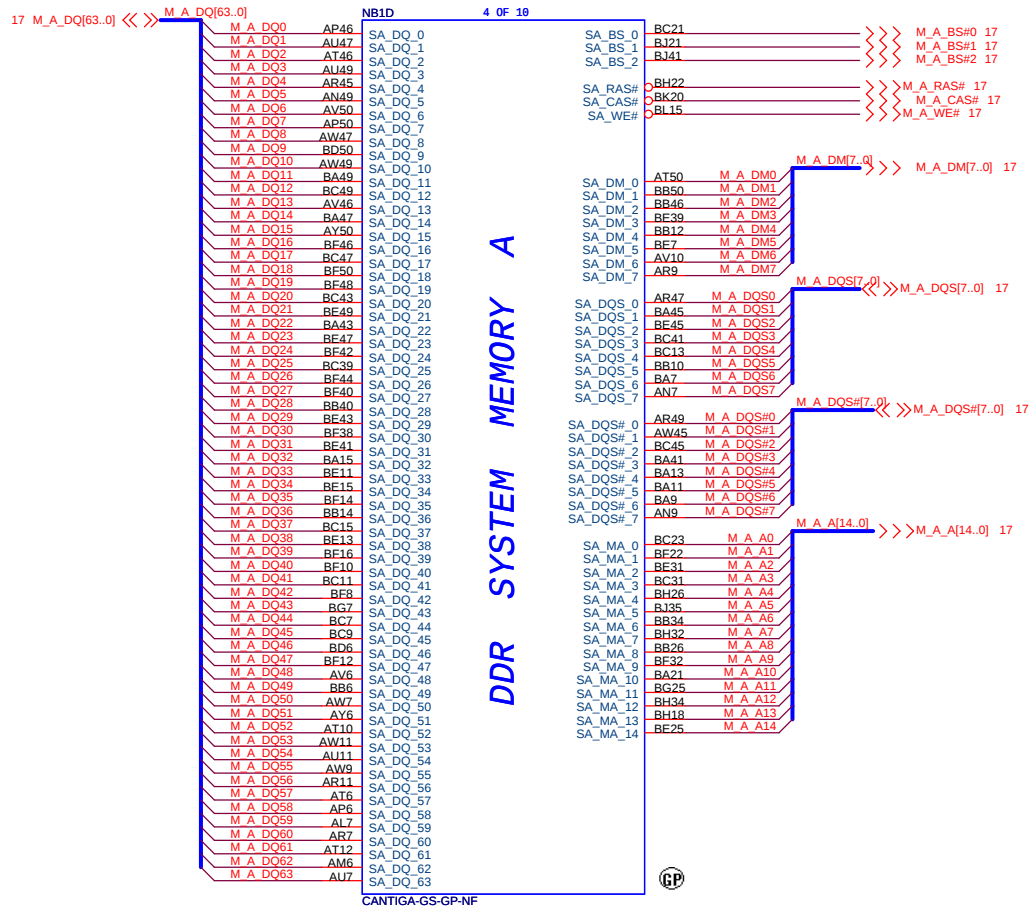
HOST

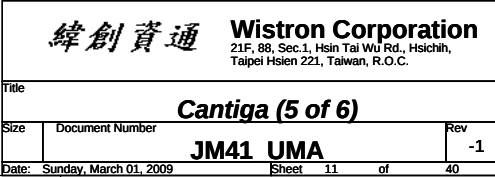


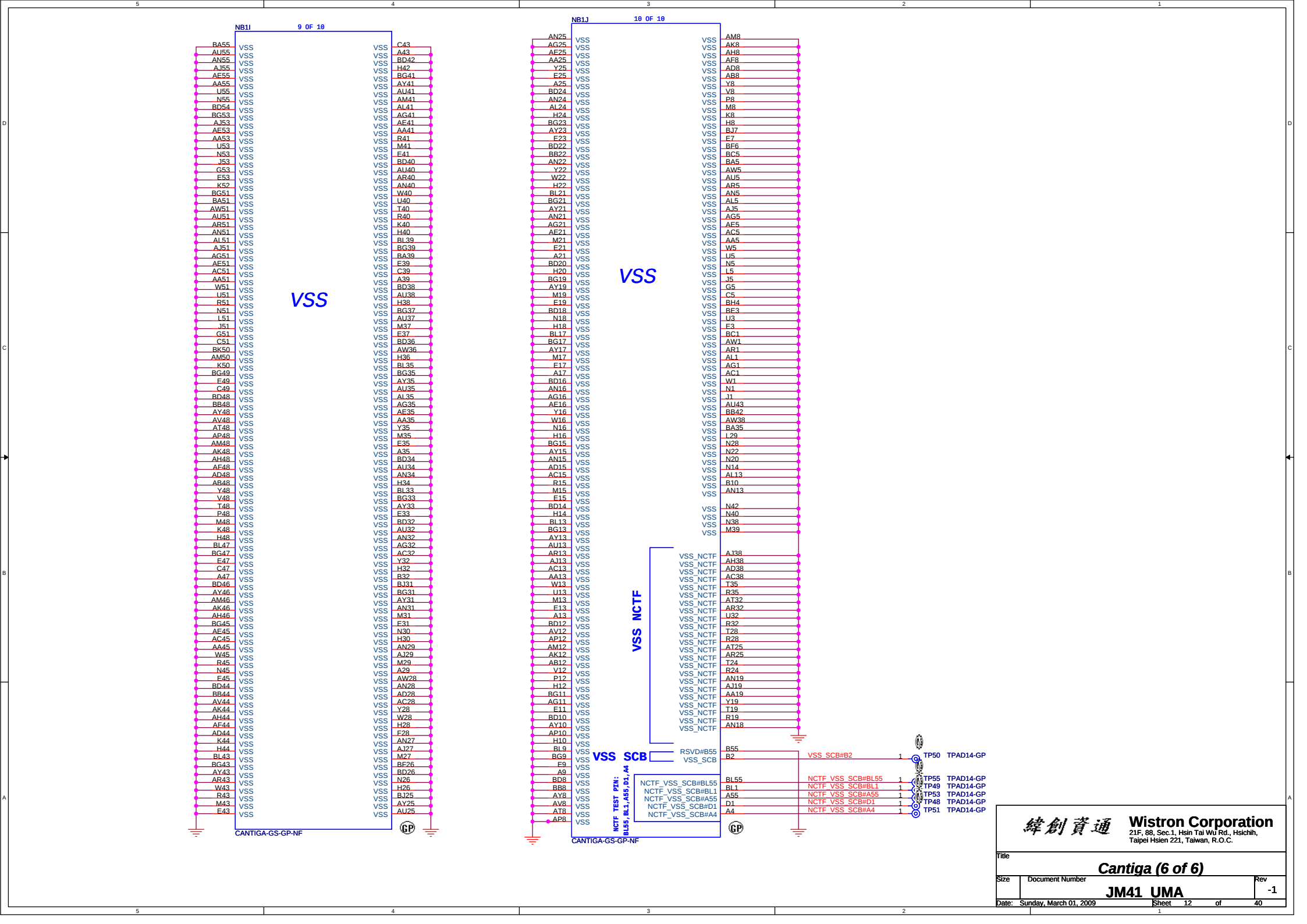
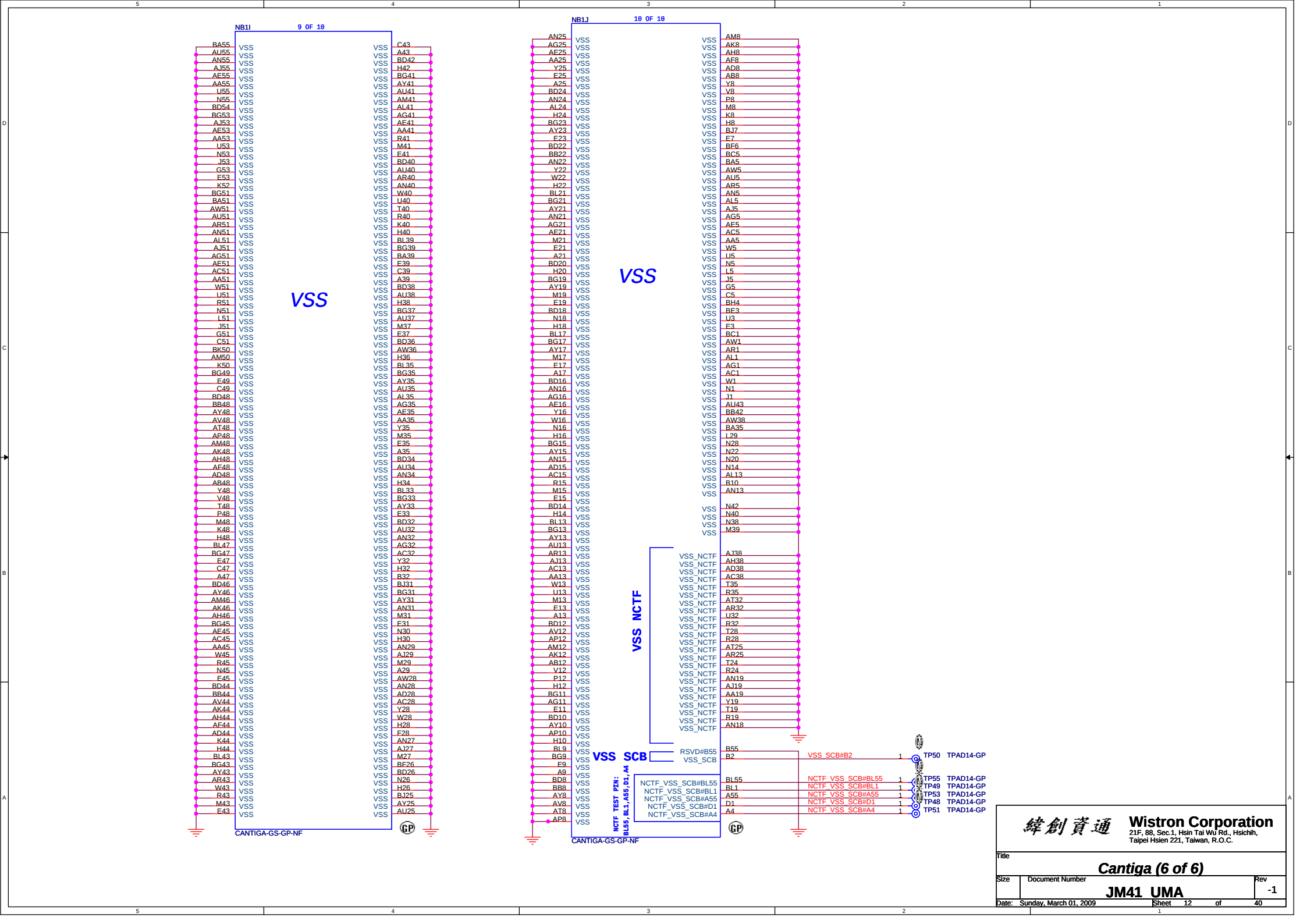
<Core Design>

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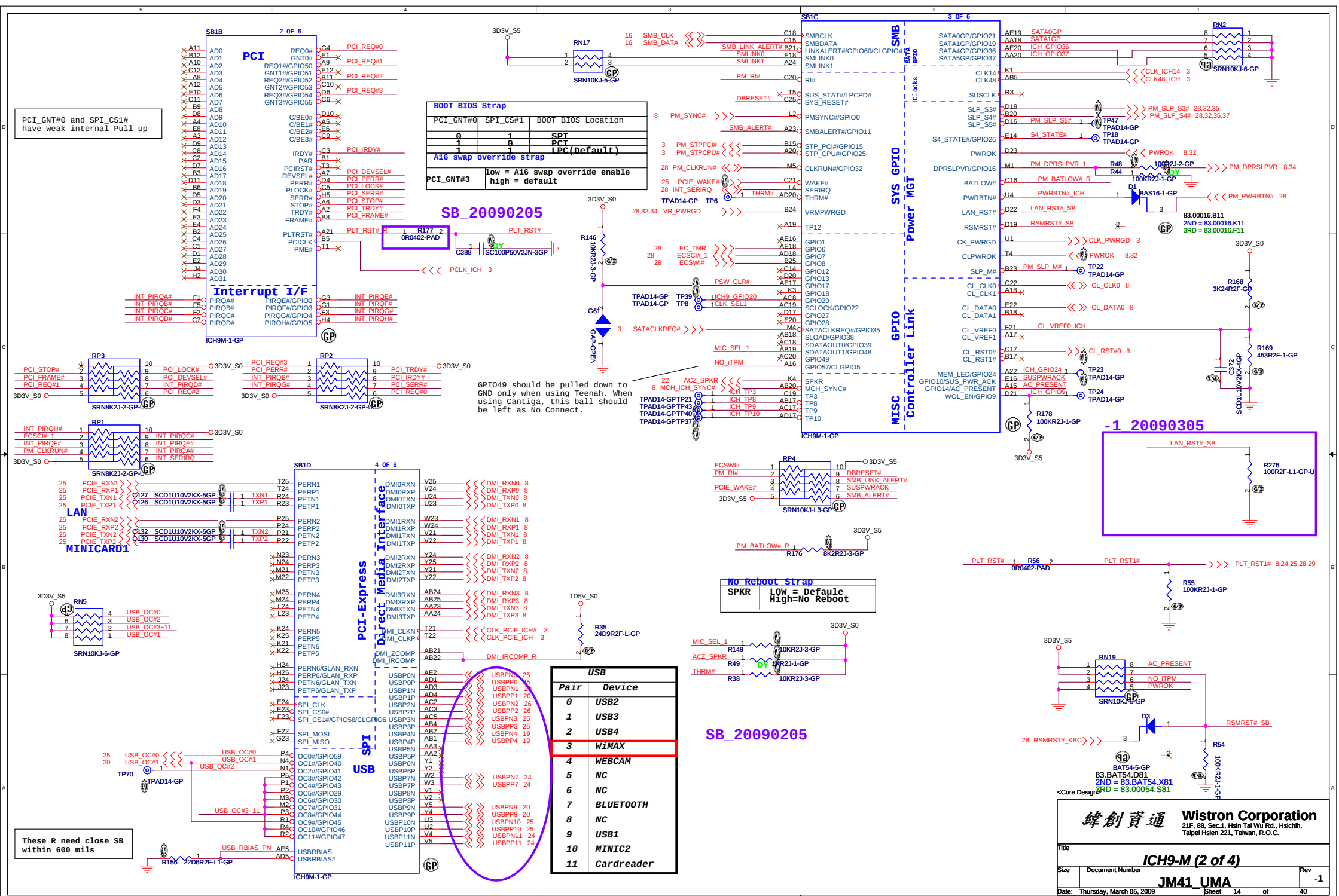


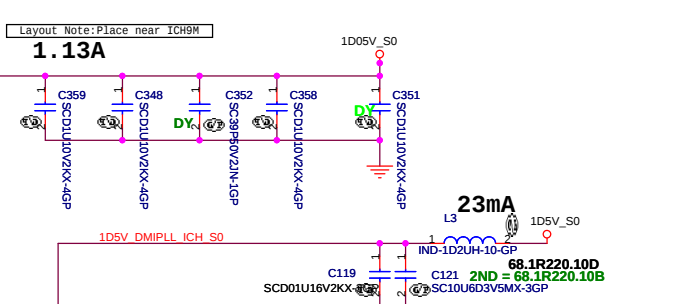
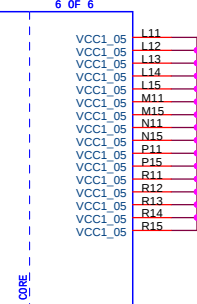
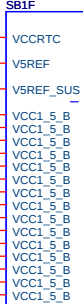
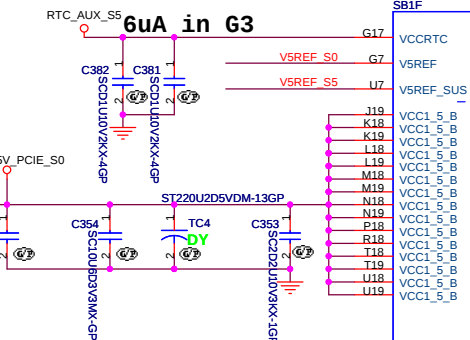
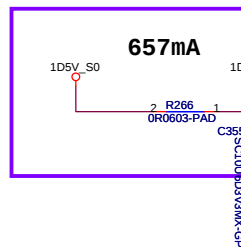






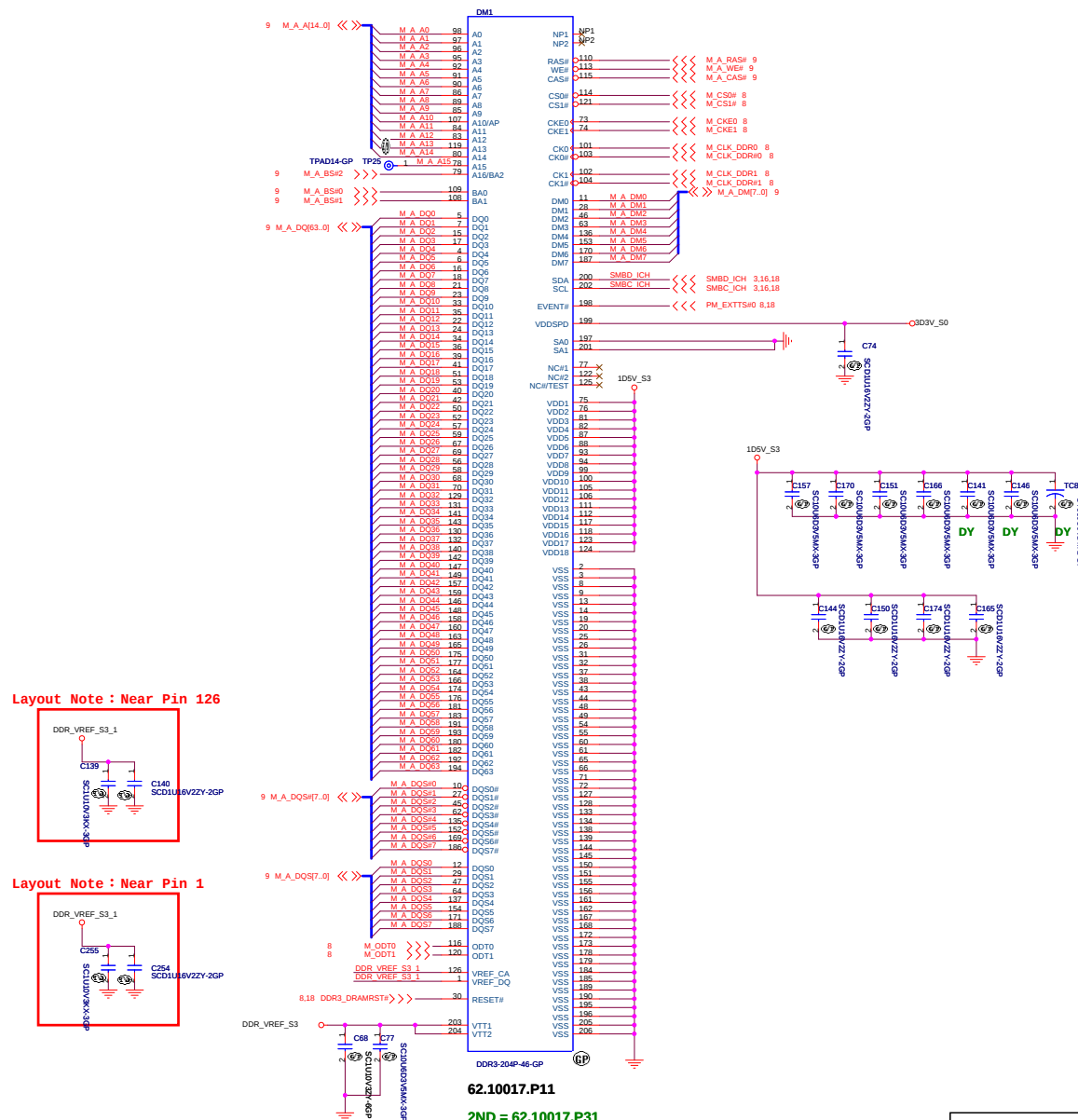




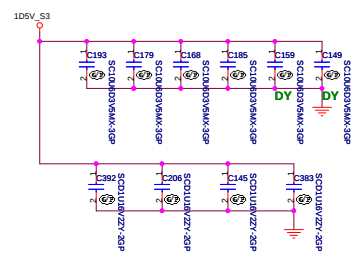




DDR3 SOCKET_1

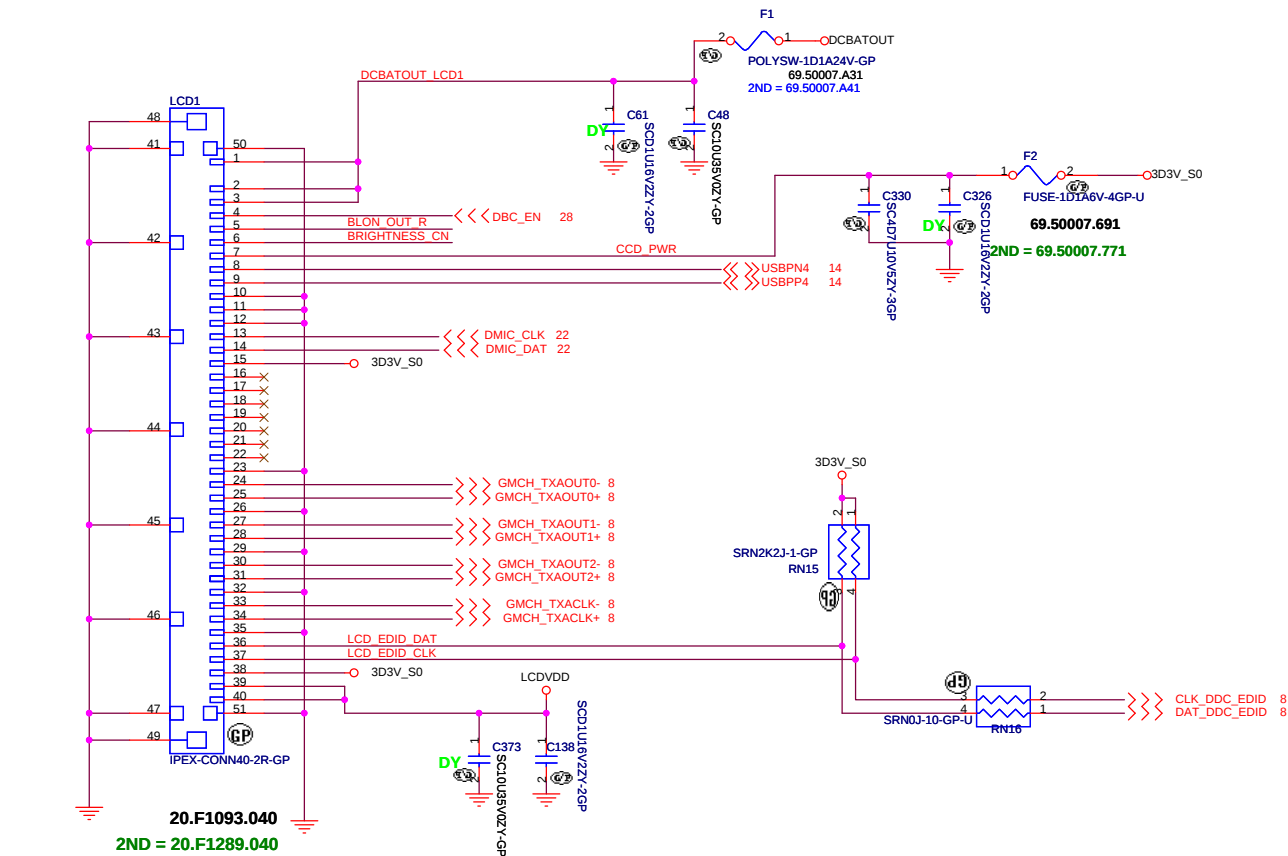


DOR3-204P-7-GP U1
62.10017.F81
2ND = 62.10017.N41

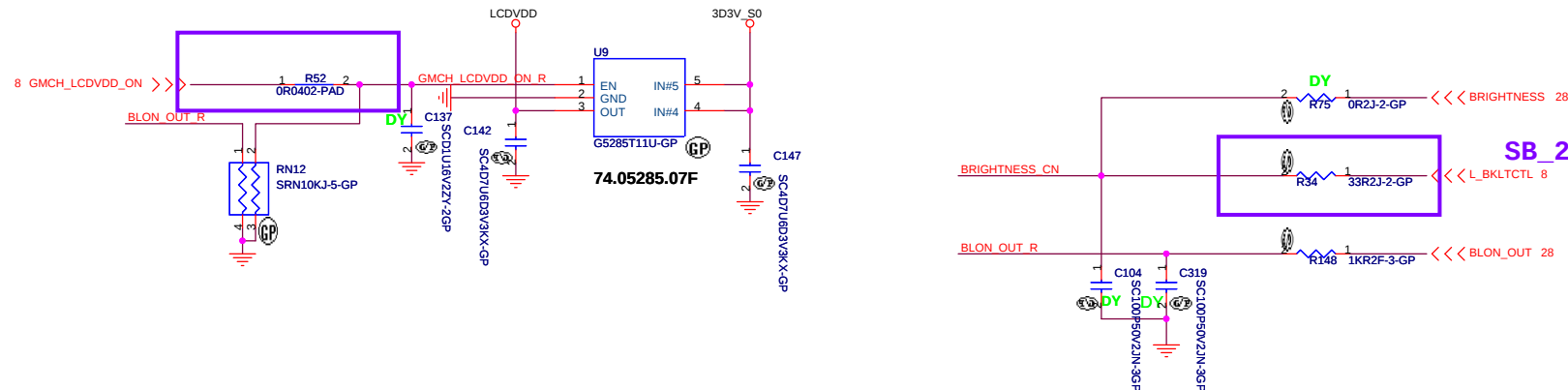


LCD/CCD CONN

Internal MIC



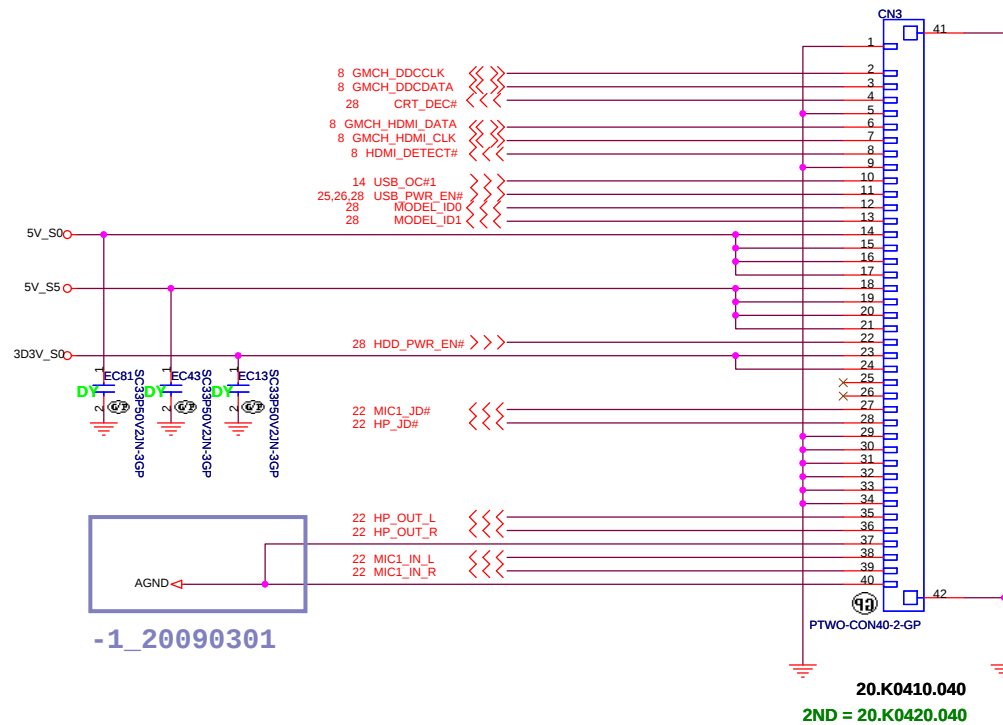
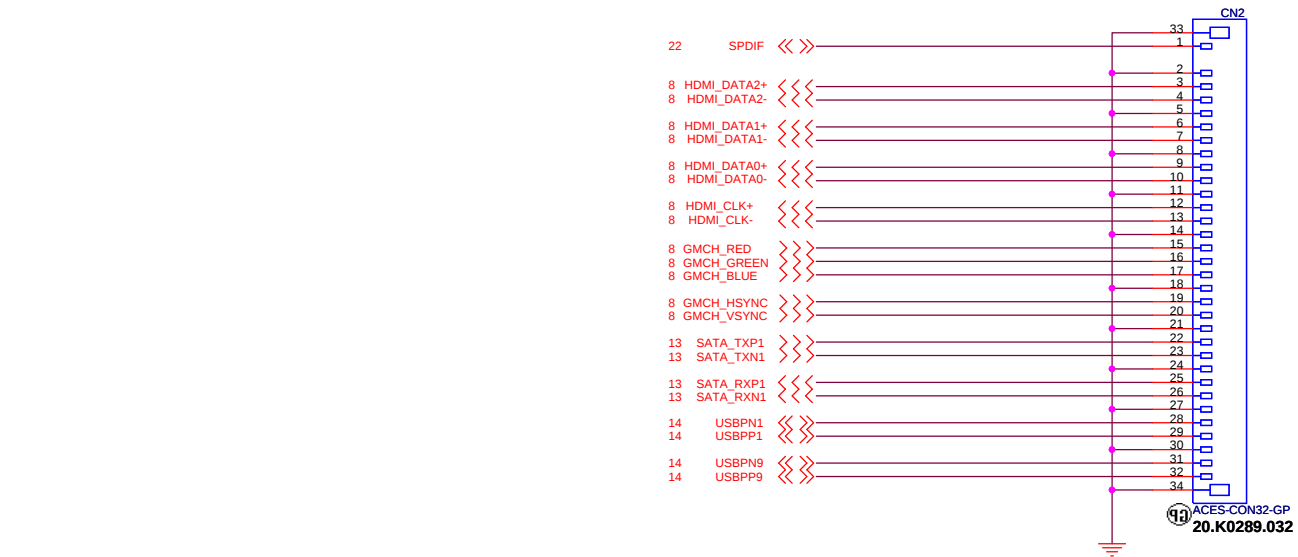
Layout 40 mil



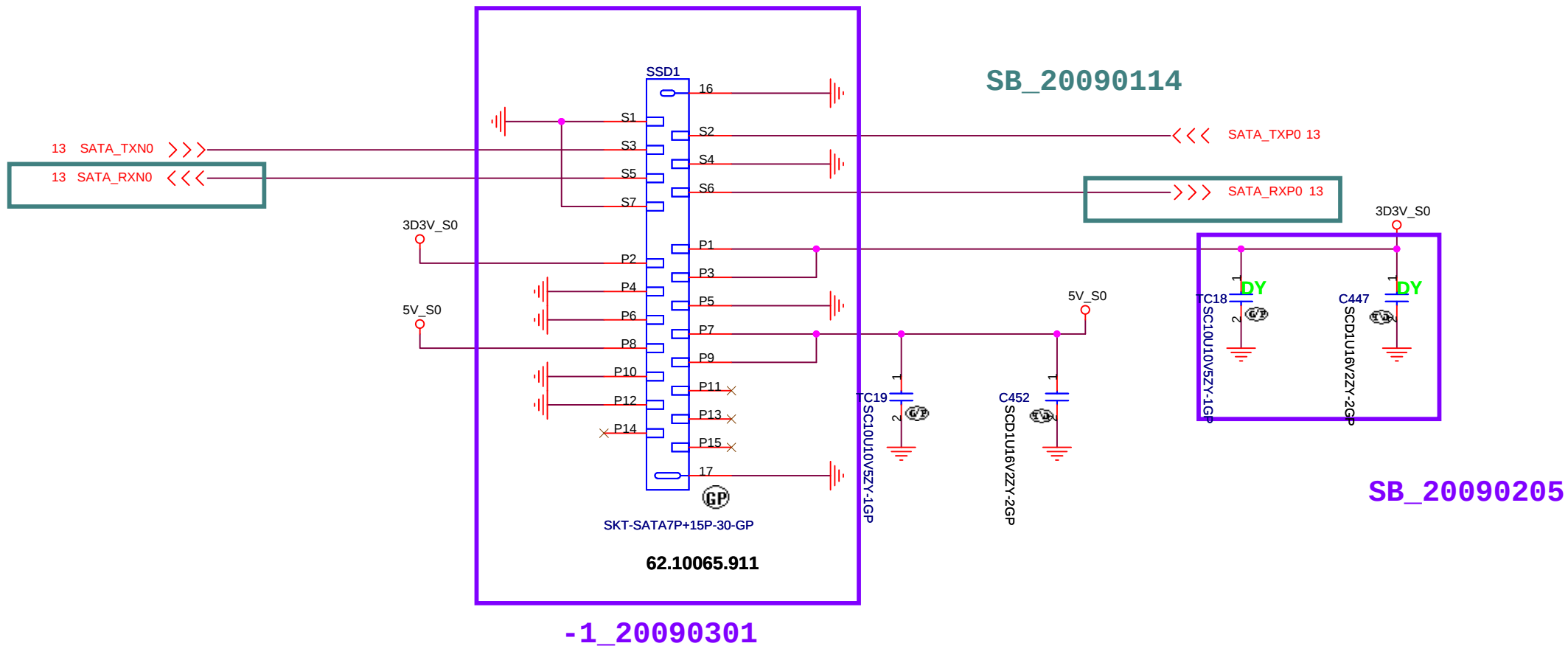
<Core Design>

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Title			
LCD CONN			
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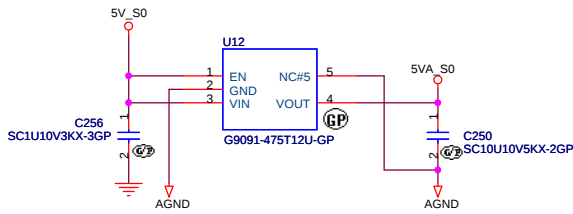


SSD SATA Connector

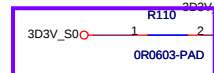


<Core Design>

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Title			
HDD CONN			
Size	Document Number		Rev
	JM41 UMA		-1
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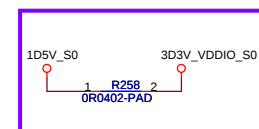
74.09091.F3F
2ND = 74.09198.A7F



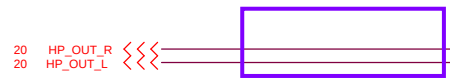
Put C735 Close To CODEC



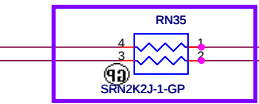
SB_20090205



SB_20090205

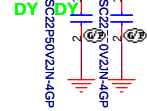
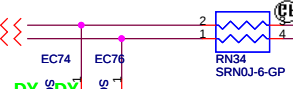
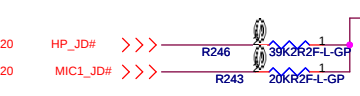


SB_20090205

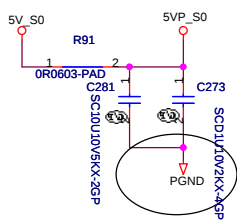
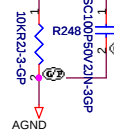
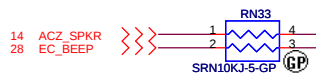


Alnalog signal

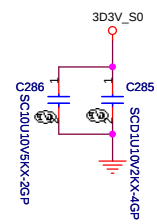
Digital signal



Put C736 Close To CODEC

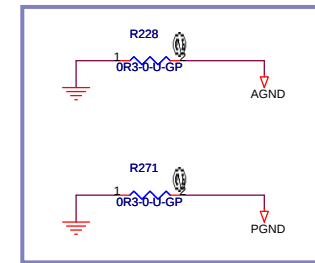


Close Pim.39
and Pin.46



Close Pim.1
and Pin.9

-1_20090301

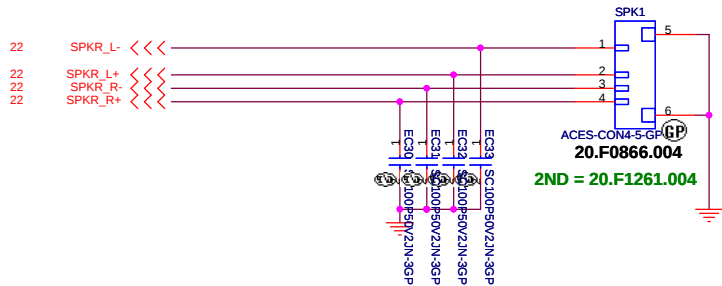


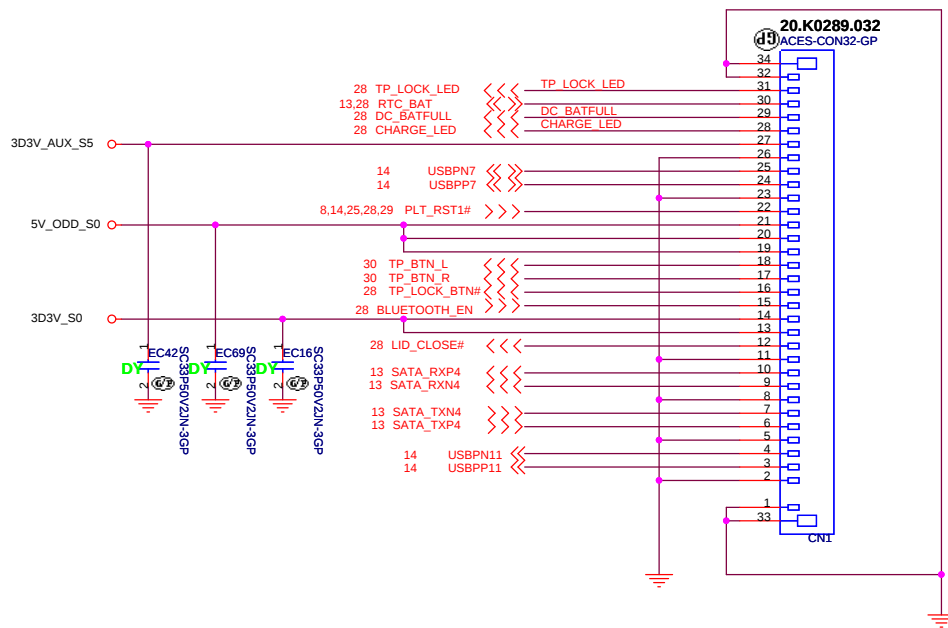
<Core Design>

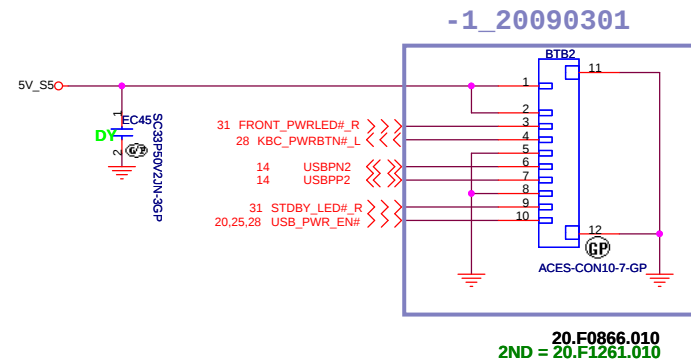
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Title		AUDIO CODEC REALTEK ALC269	
Size	Document Number	JM41 UMA	Rev -1
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Internal Speaker

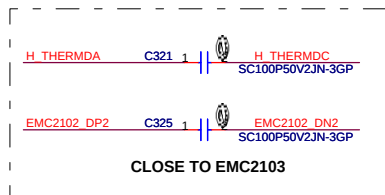






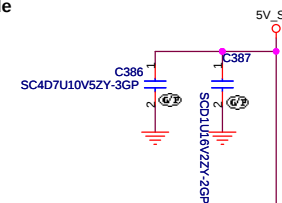
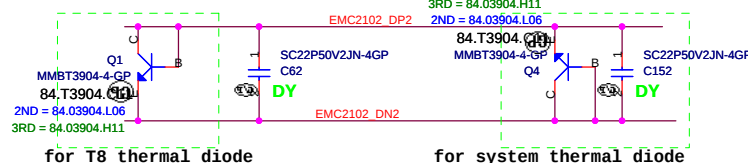
<Core Design>

Title		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Size A3		Document Number JM41_UMA	
Date: Thursday, March 05, 2009		Sheet 26 of 40	
Rev -1			

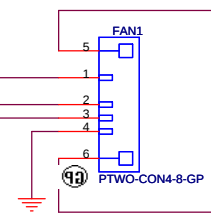


CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near thermal diode

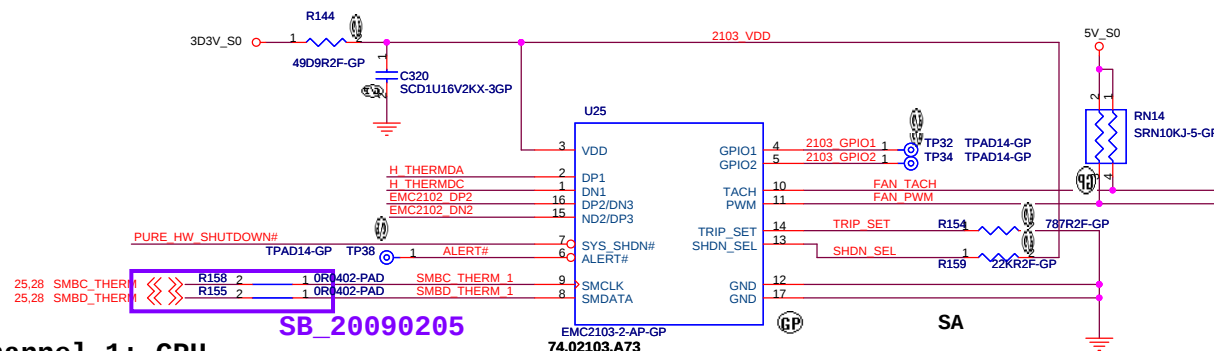
for CPU thermal diode



C587 for EMI and solve acoustic noise



20.F1396.004
2ND = 20.F0411.004



ps. FAN1 POWER TRACE WIDTH MAY BE IN 25 MIL

Channel 1: CPU
Channel 2: Palmrest
Channel 3: T8

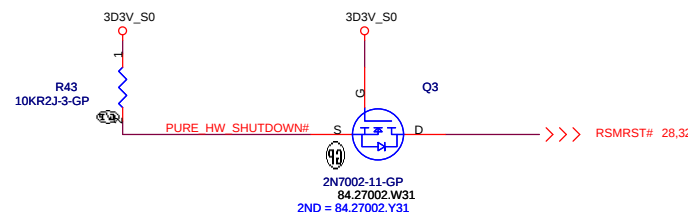
SB_20090205

SHDN SEL

PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED, REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED, REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED

TRIP SET

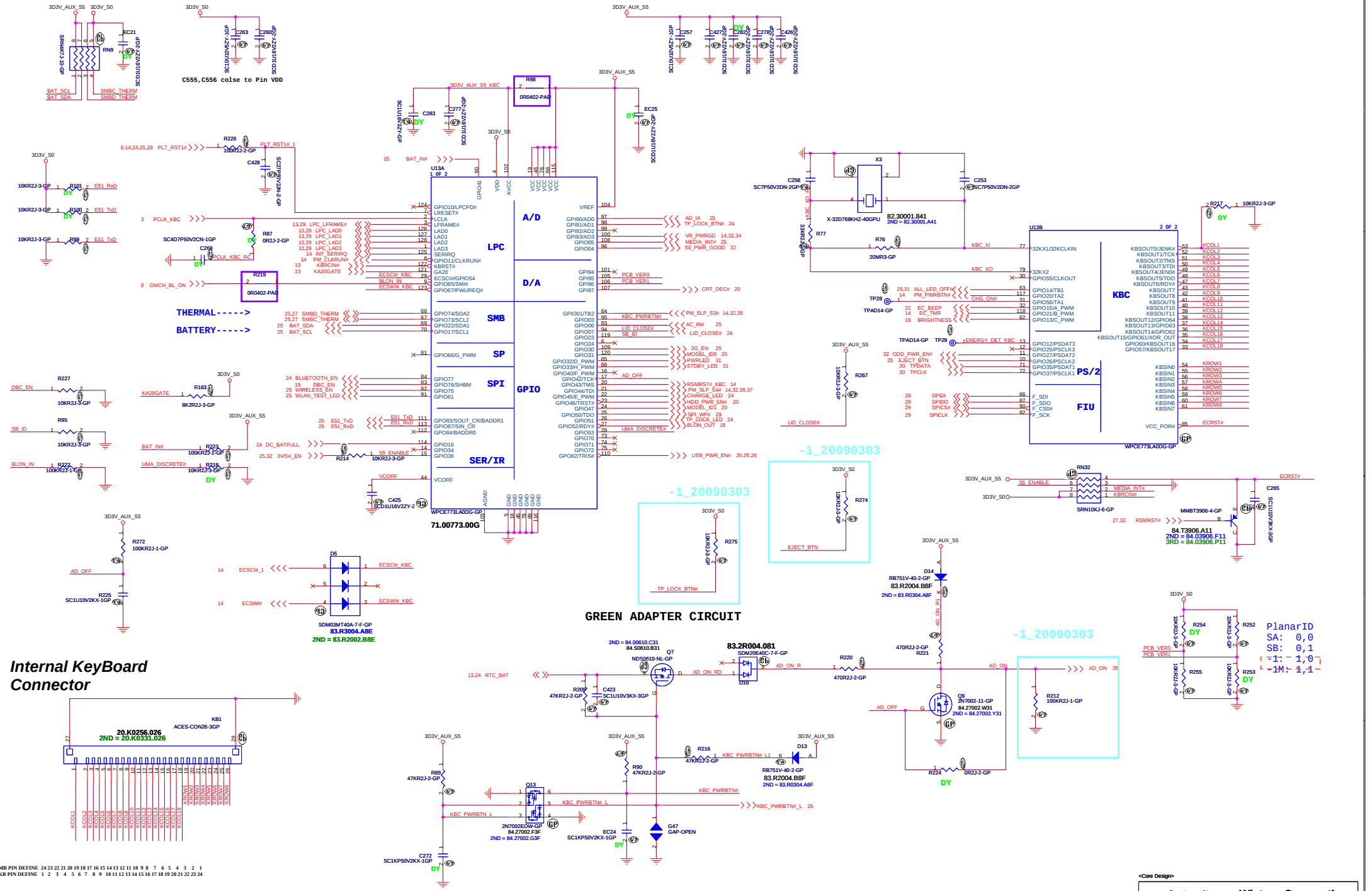
Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100



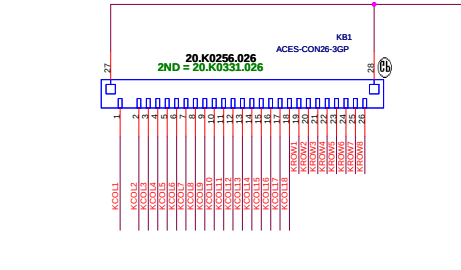
<Core Design>

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Title	Thermal/Fan Controllor	Rev	-1
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Date: Thursday, March 05, 2009	JM41 UMA	Sheet 27 of 40	



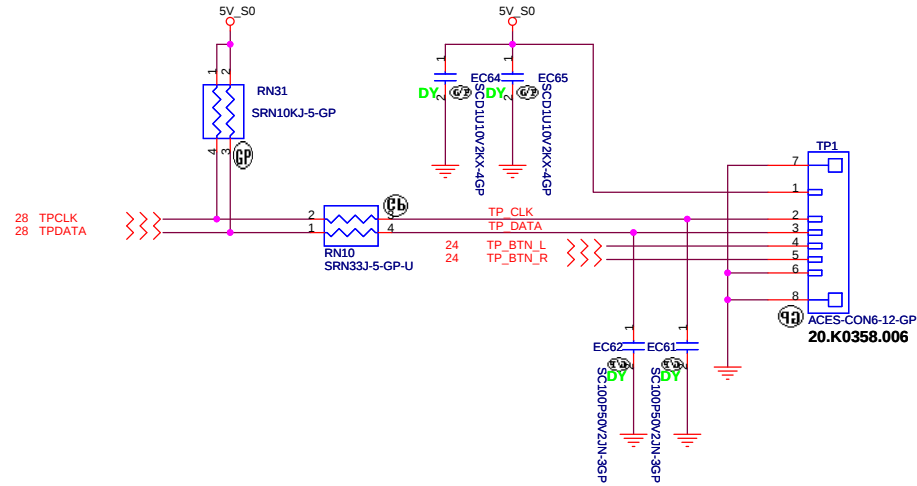
Internal Keyboard Connector



MB PIN DEFINE: 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

24 K/B 1

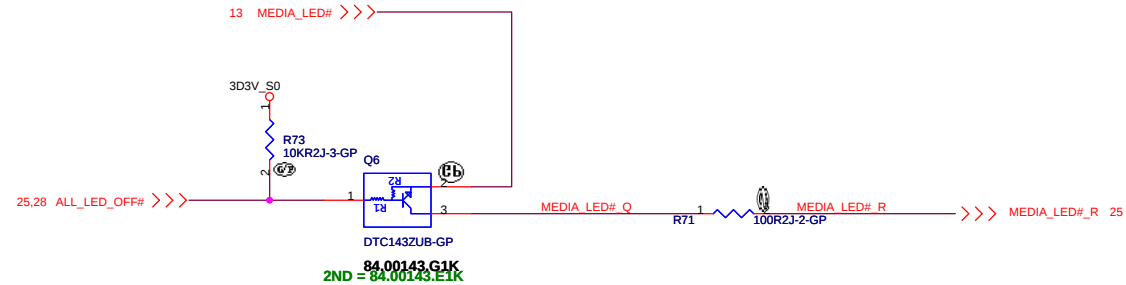
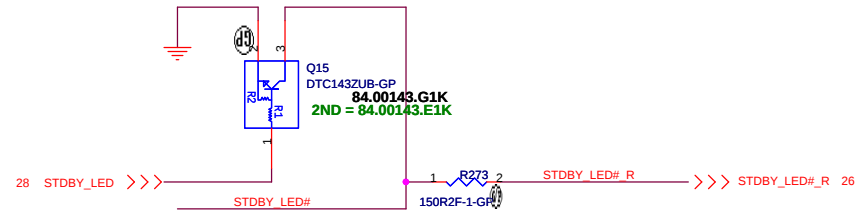
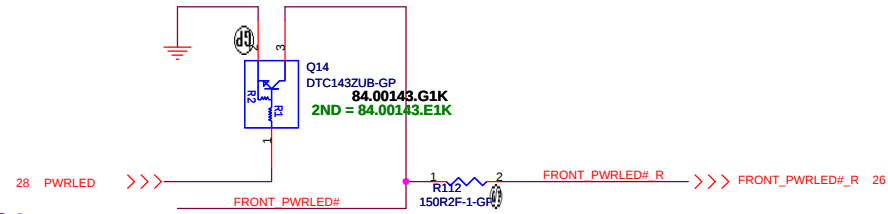
TOUCH PAD



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Title			
Touch PAD			
Size	Document Number		Rev
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-1_20090301

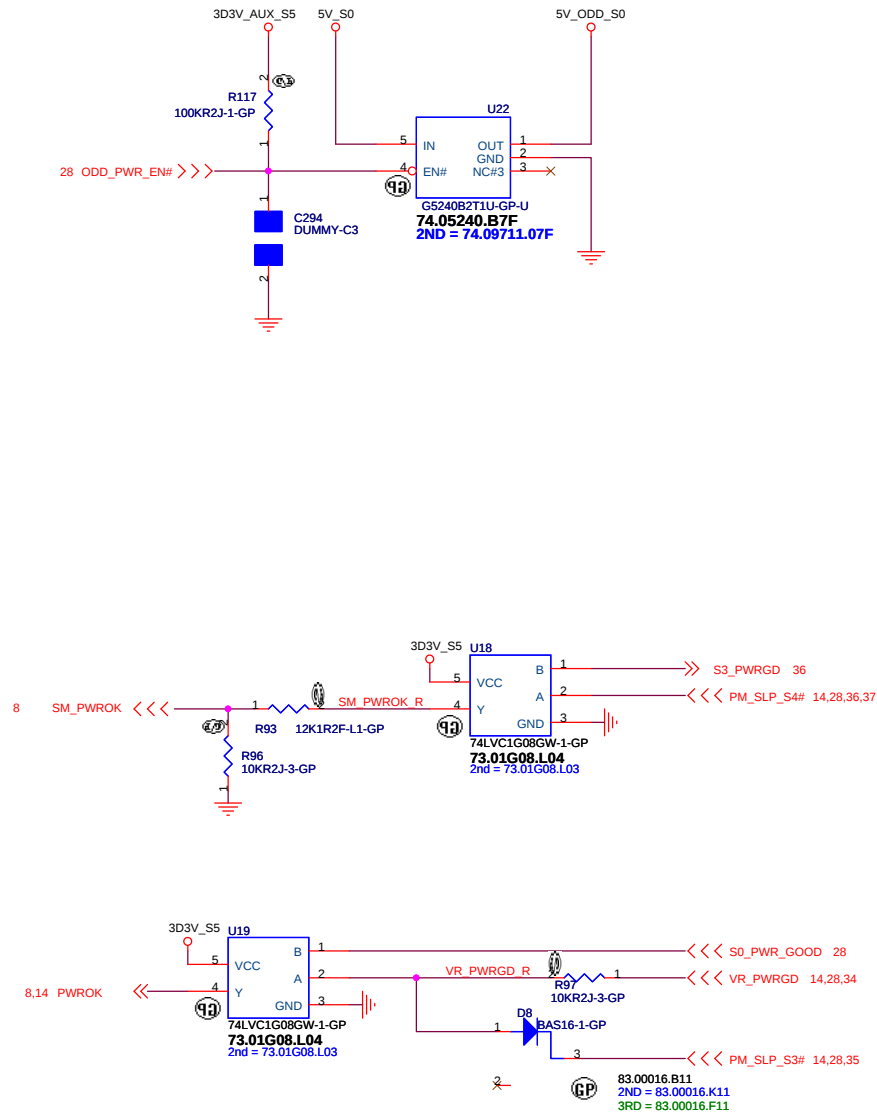


<Core Design>

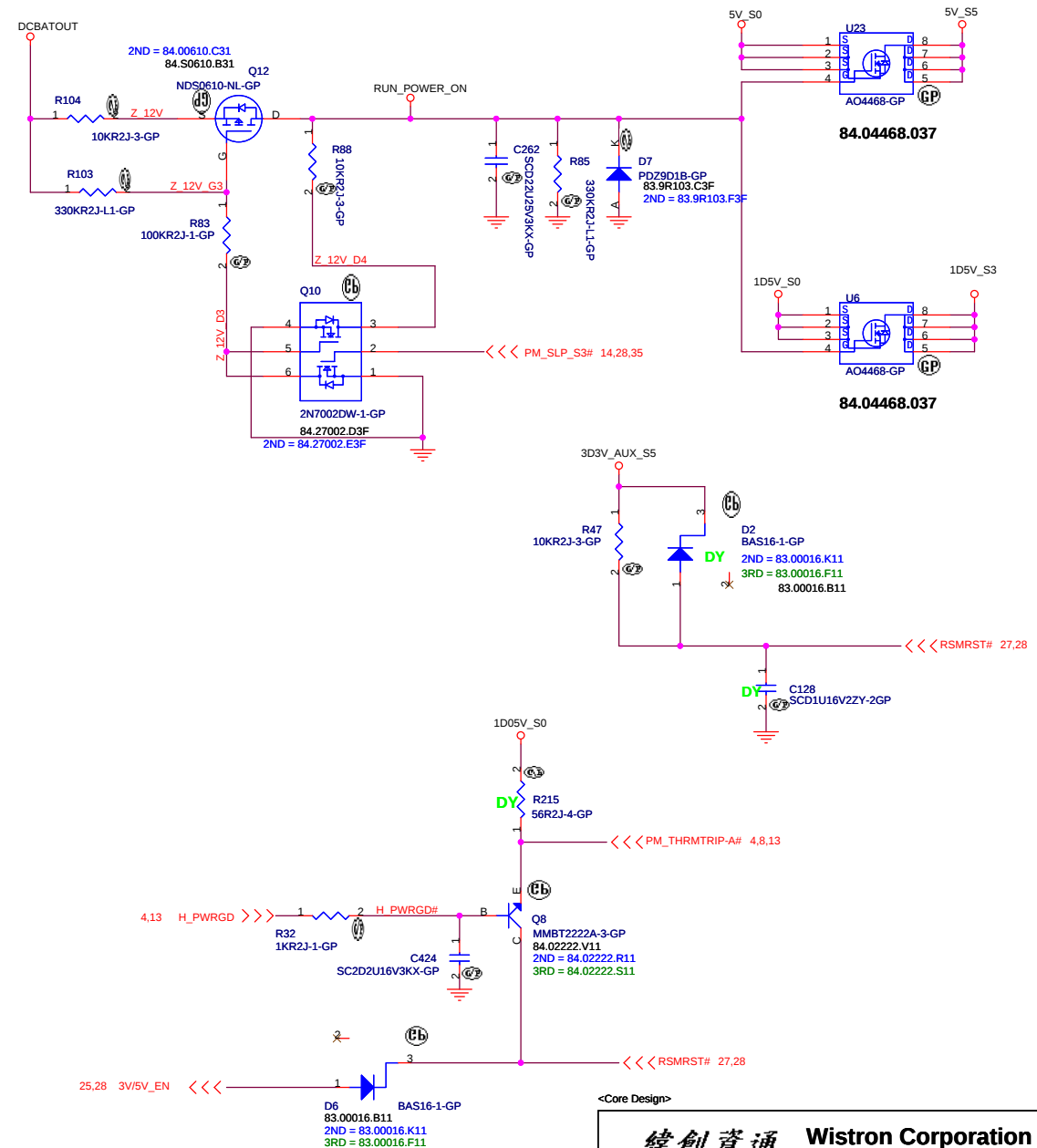
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

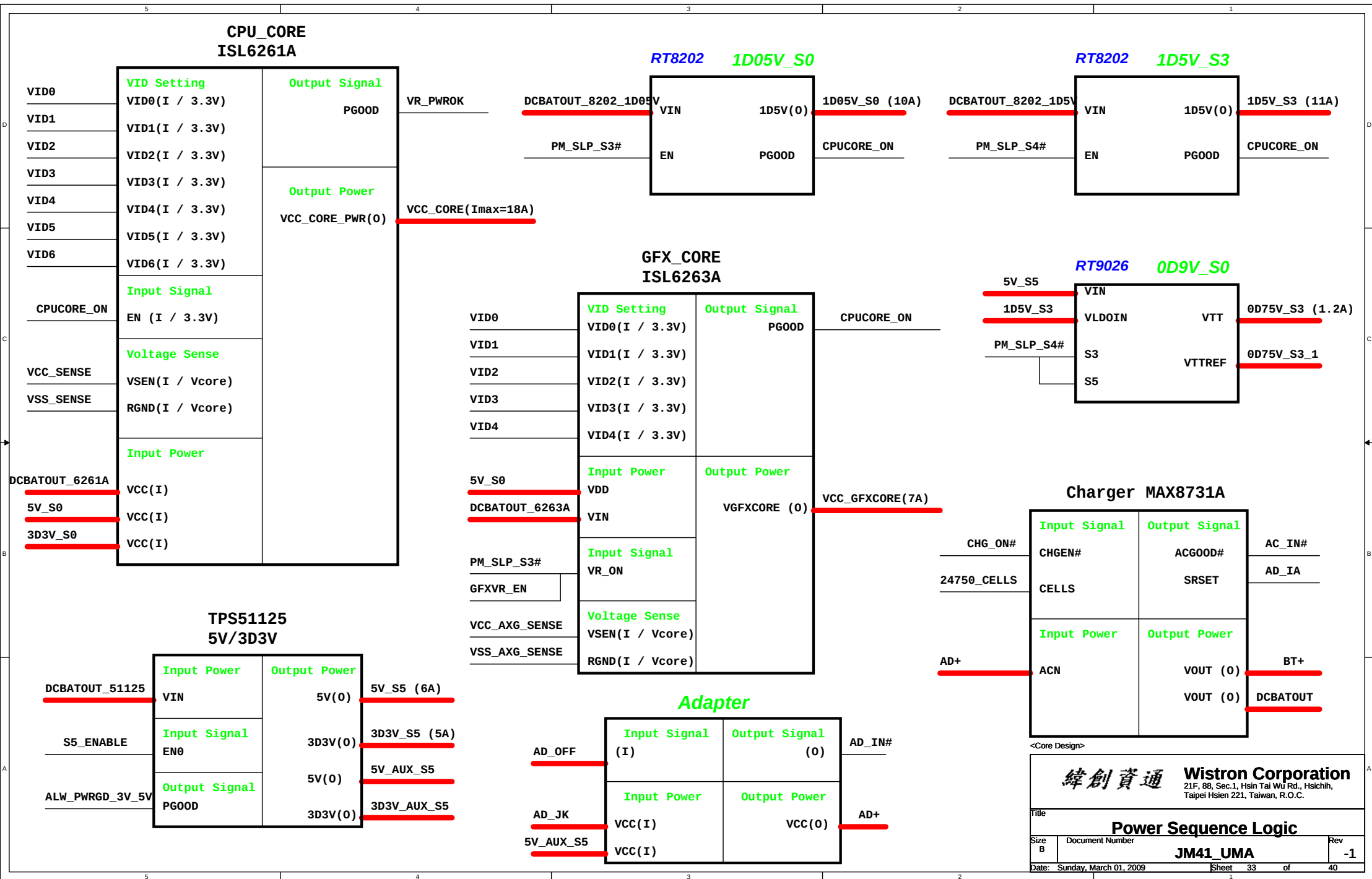
Title		LED	
Size	Document Number	JM41_UMA	Rev
Date: Thursday, March 05, 2009		Sheet 31 of 40	-1

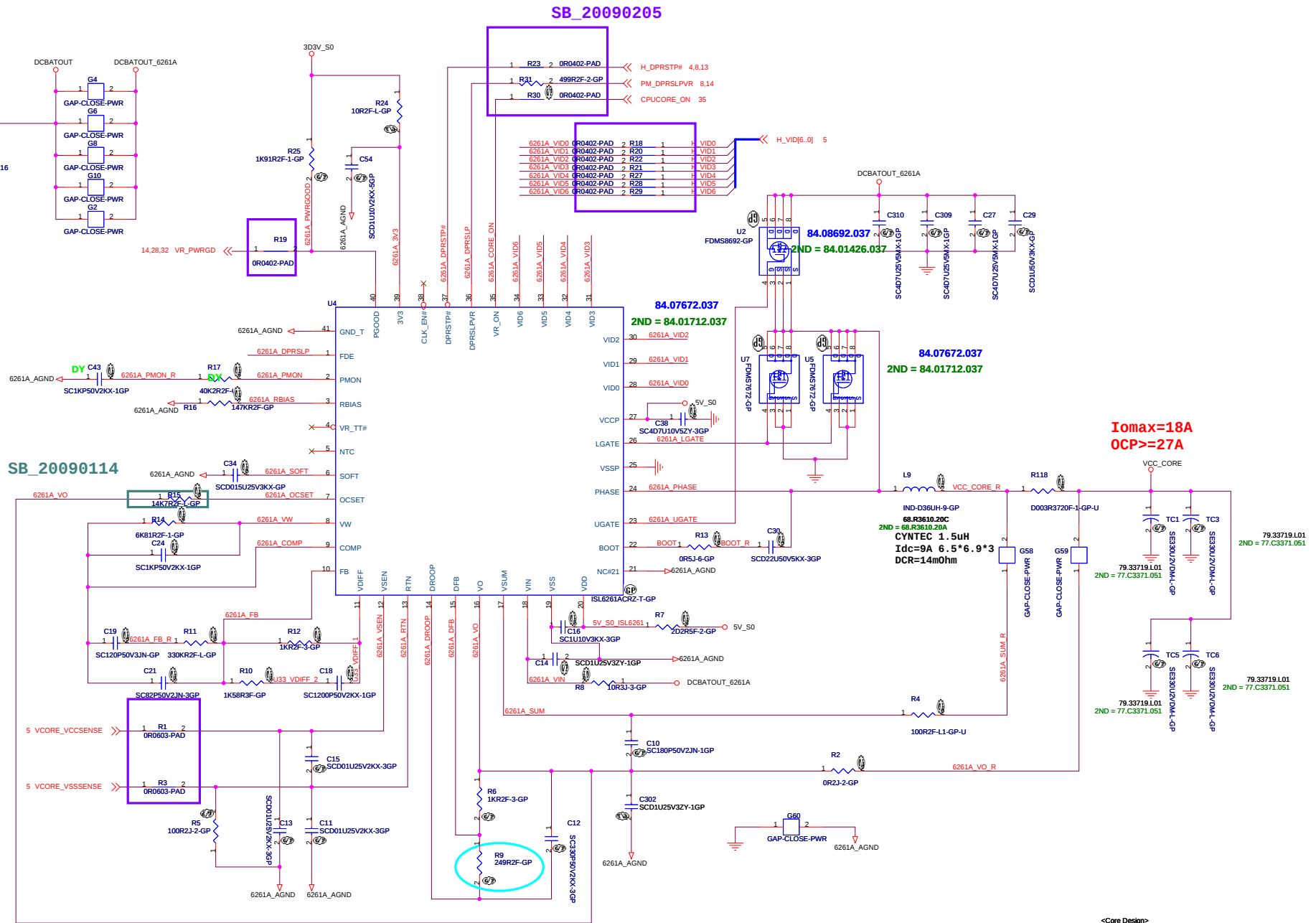
ODD Power



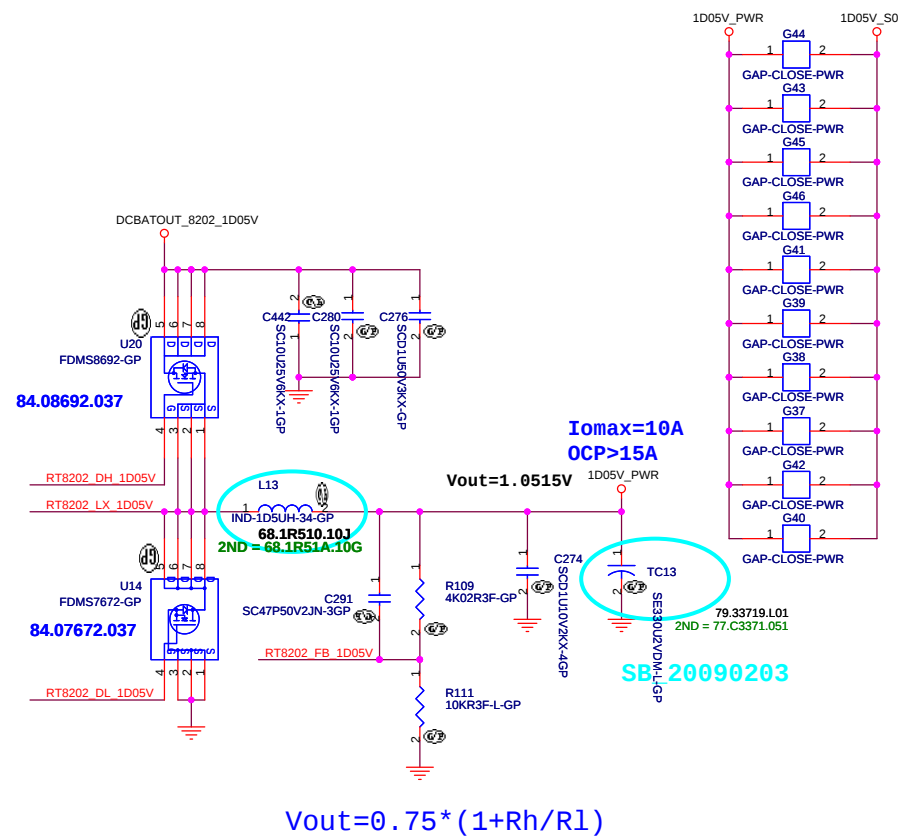
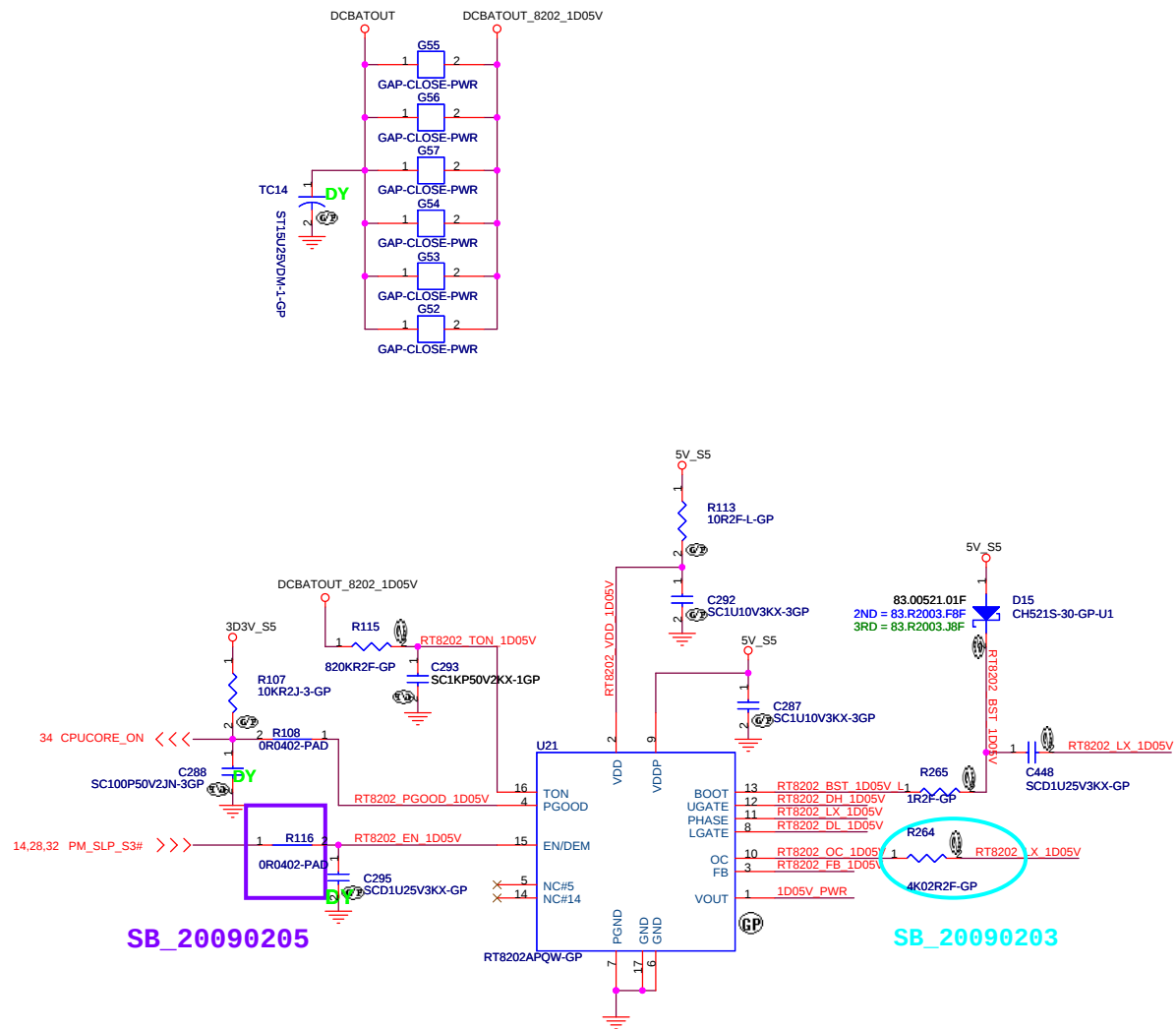
Run Power







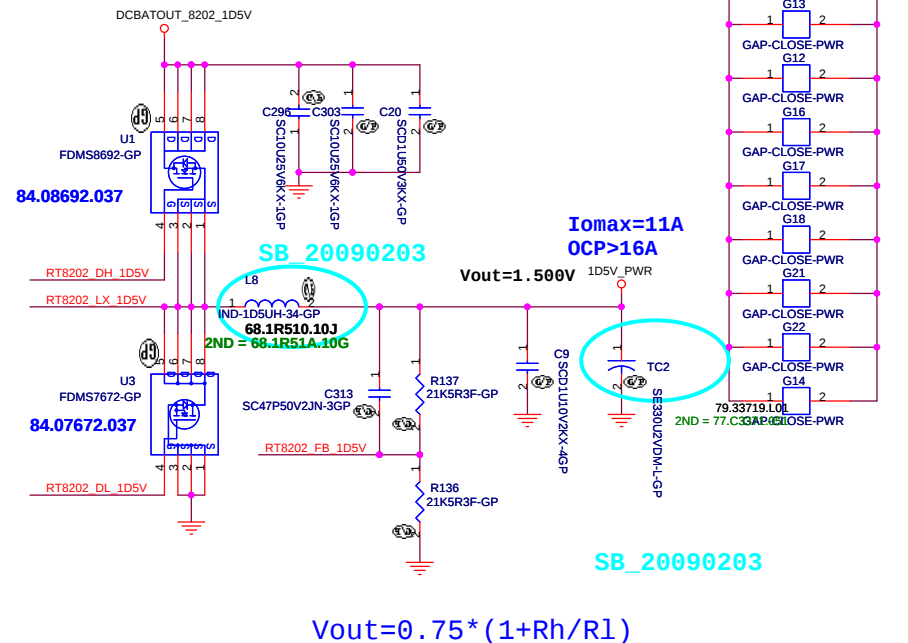
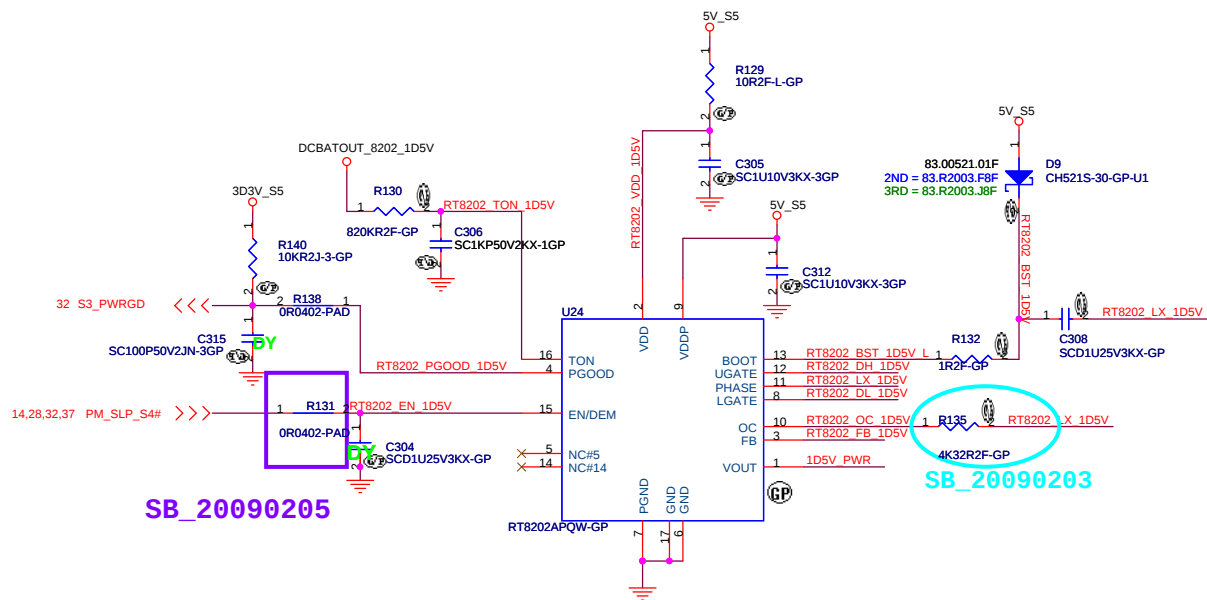
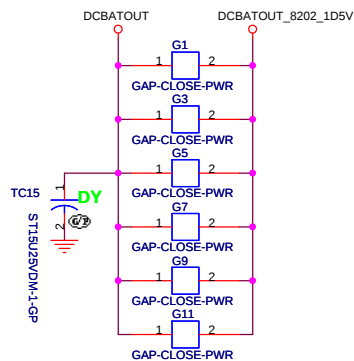
Iomax=18A
OCP>=27A

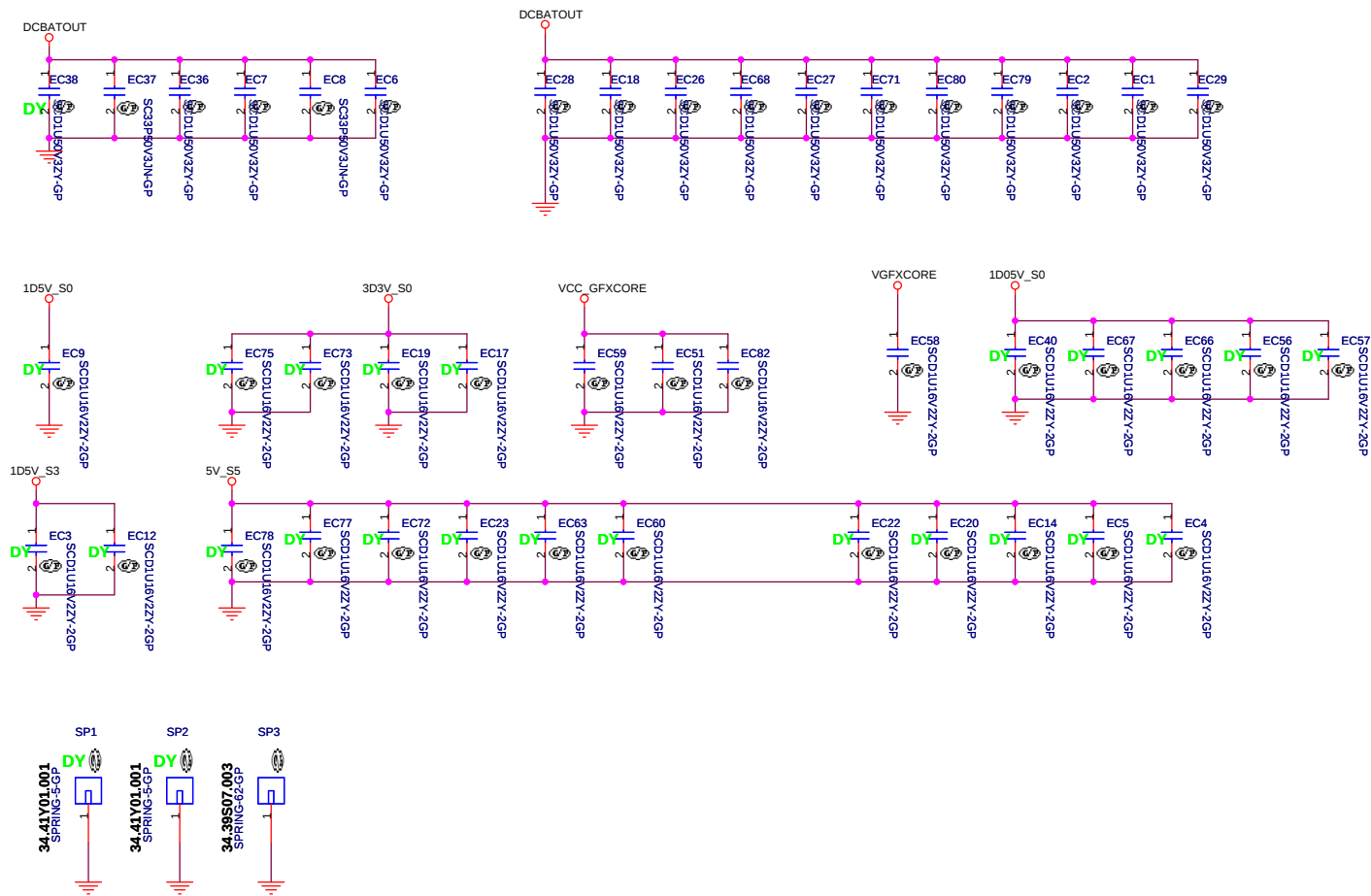


<Core Design>

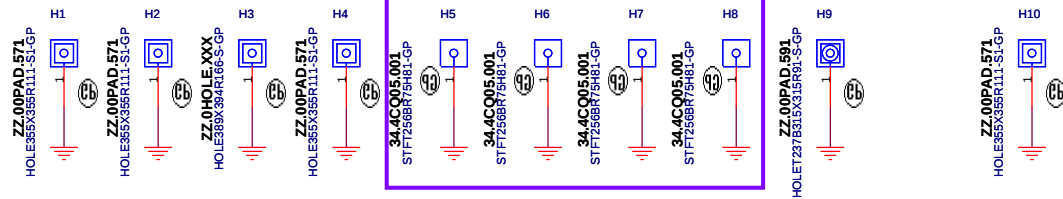
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Taipei Hsien 221, Taiwan, R.O.C.

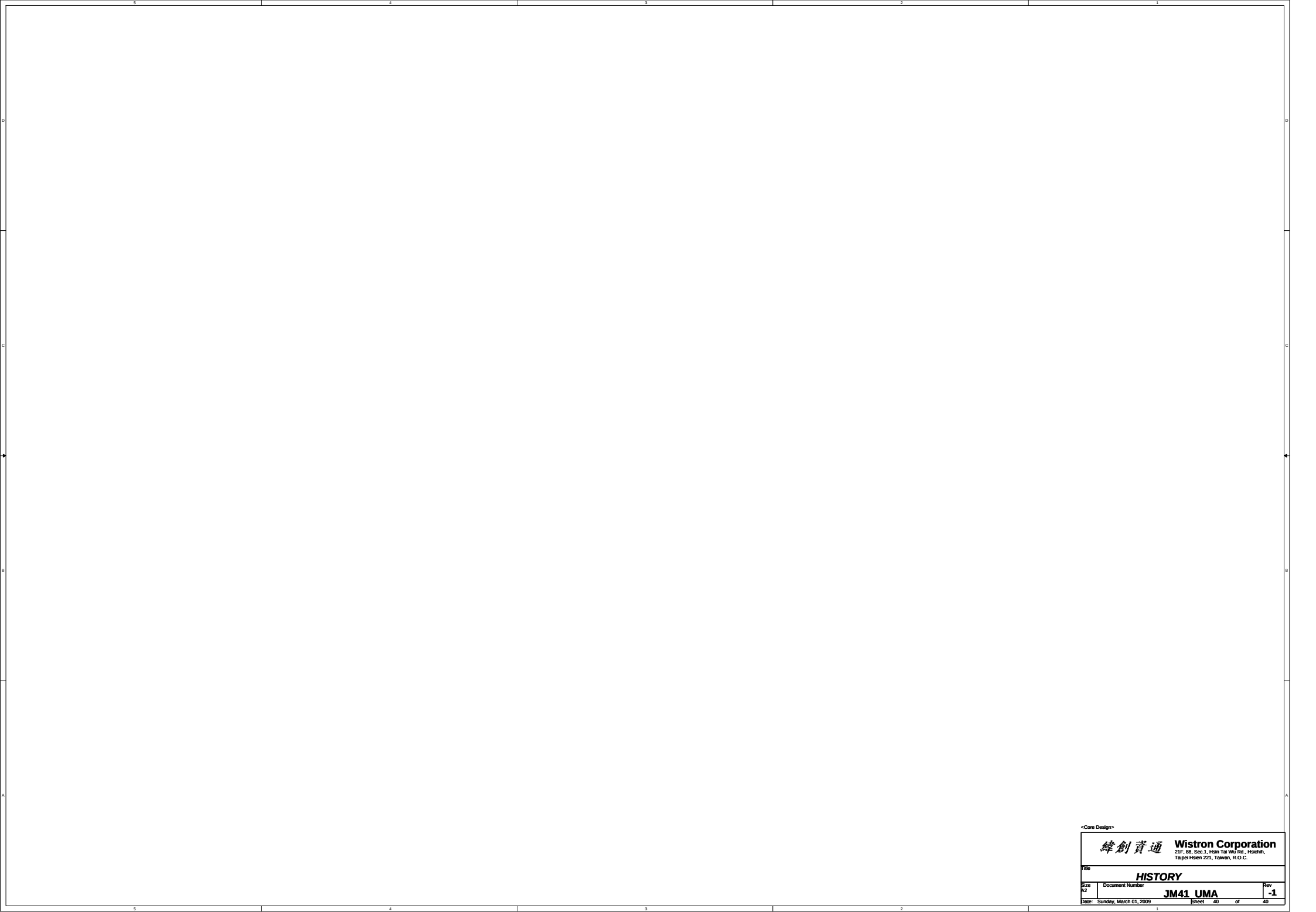
Title		RT8202 1D05V	
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SB_20090115





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Title			
HISTORY			
Size A2	Document Number JM41 UMA		Rev -1
Date: Sunday, March 01, 2009		Sheet 40 of 40	